WHAT IS CLAIMED IS:

1. A CAM circuit comprising:

a memory unit connected to a word line and a bit line;

a data compare unit connected to a match line and a compare line, the data compare unit comparing a data stored in the memory unit to a data of the compare line in a state where the match line is activated;

a consistency cancel circuit provided in each word line and each match line, the consistency cancel circuit forcibly making the match line inactive when the word line and a write instruction signals are both activated.

2. The CAM circuit according to Claim 1, further comprising:

a column select circuit for selecting the bit line in accordance with a column selection signal; and

a consistency cancel control circuit for generating and outputting a consistency cancel / select signal to the consistency cancel circuit in accordance with a combination of the write instruction signal and the column selection signal.

3. The CAM circuit according to Claim 1, further comprising:

a write data compare circuit for comparing a signal of a path before a write data is written in the memory unit to a retrieval data outside the memory unit; and

a restoration regulating circuit for denying an output of a forcible inconsistency by the consistency cancel circuit at a write address when a result of the comparison by the write data compare circuit shows consistency.

4. A CAM circuit comprising:

a CAM memory cell comprising a CAM memory unit connected to a word line and a bit line;

a data compare unit connected to a match line and a compare line in order to compare a data stored in the CAM memory unit to a data in the compare line in a state where the match line is activated;

a mask memory cell comprising a mask bit line, the word line shared with the CAM memory unit and a mask memory unit, wherein the mask memory cell has a role to stop the operation of the data compare unit in the active state;

a consistency cancel circuit for changing a value of the match line according to a value of a write instruction signal and the word line;

a write data compare circuit for comparing a signal of a path before a write data is written in the memory unit to a retrieval data outside the memory unit; and

a restoration regulating circuit for denying an output of a forcible inconsistency by the consistency cancel circuit at a write address when a result of the comparison by the write data compare circuit shows consistency.

5. An output method of a CAM circuit comprising:

a memory unit connected to a word line and a bit line; and

a data compare unit connected to a match line and a compare line, which has a role to compare a data stored in the memory unit to a data of the compare line in a state where the match line is activated, wherein

a state of the corresponding match line is forcibly made to be inconsistent in the case of detecting that the word line and a write instruction signal are both in an enable state when a write operation and a retrieve operation are both instructed based on an identical clock cycle.

6. The output method of a CAM circuit according to Claim 2, wherein the corresponding match line is made to be inconsistent in the case of detecting that the write instruction signal, the word line and the column selection signal are all in the enable state when a write operation with respect to the memory and a retrieve operation are both instructed based on an identical clock cycle.

7. The output method of a CAM circuit according to Claim 5, wherein a signal of a path before a write data is written in the memory unit and a retrieval data are compared to each other outside the memory unit when the write operation to the memory and the retrieve operation are both instructed based on the identical clock cycle, and a consistency detection result at a write address is changed from inconsistency to consistency according to a result of the comparison.

8. An output method of a CAM circuit comprising:

a CAM memory cell comprising a CAM memory unit connected to a word line and a bit line;

a data compare unit connected to a match line and a compare line, which has a role to compare a data stored in the CAM memory unit to a data in the compare line in a state where the match line is activated;

a mask memory cell comprising a mask bit line, the word line shared with the CAM memory unit and a mask memory unit, which has a role to stop the operation of the data compare unit in the active state;

a consistency cancel circuit for changing a value of the match line according to a write instruction signal and a value of the word line; and

a write data compare circuit for comparing a signal of a path before a write data is written in the memory unit to a retrieval data outside the memory unit, wherein

a state of the corresponding match line is forcibly made to be inconsistent in the case of detecting that the word line and a write instruction signal are both in an enable state when a write operation and a retrieve operation are both instructed based on an identical clock cycle, the signal of the path before the write data is written in the memory unit and the retrieval data are compared to each other outside CAM memory unit and the mask memory unit, and a consistency detection result at

a write address is changed from inconsistency to consistency according to a result of the comparison.